| Notice of References Cited | Application/Control No.<br>09/733,254 | Applicant(s)/Patent Under Reexamination<br>GRANSTON ET AL. | |
|---|---|---|---|
| | Examiner<br>Tuan A Vu | Art Unit<br>2124 | Page 1 of 1 |

**U.S. PATENT DOCUMENTS**

| * | | Document Number<br>Country Code-Number-Kind Code | Date<br>MM-YYYY | Name | Classification |
|---|---|---|---|---|---|
| | A | US-6,240,509 | 05-2001 | Akkary, Haitham | 712/228 |
| | B | US-5,930,492 | 07-1999 | Lynch, Thomas W. | 712/216 |
| | C | US- | | | |
| | D | US- | | | |
| | E | US- | | | |
| | F | US- | | | |
| | G | US- | | | |
| | H | US- | | | |
| | I | US- | | | |
| | J | US- | | | |
| | K | US- | | | |
| | L | US- | | | |
| | M | US- | | | |

**FOREIGN PATENT DOCUMENTS**

| * | | Document Number<br>Country Code-Number-Kind Code | Date<br>MM-YYYY | Country | Name | Classification |
|---|---|---|---|---|---|---|
| | N | | | | | |
| | O | | | | | |
| | P | | | | | |
| | Q | | | | | |
| | R | | | | | |
| | S | | | | | |
| | T | | | | | |

**NON-PATENT DOCUMENTS**

| * | | Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages) |
|---|---|---|
| | U | Schlansker et al., "Achieving High Levels of Instructions-Level Parallelism with Reduced Hardware Complexity", Nov 1994, HPL-96-120, www.hpl.hp.com/techreports/96/HPL-96-120.pdf |
| | V | Rau et al., "Code Generation Schema for Modulo Scheduled Loops", ACM Proceedings of the 25th annual International Symposium on Microarchitecture, Dec 1992, volume 23, iss. 1-2 |
| | W | Rau et al., "Register Allocation for Software Pipelined Loops", June 1992, In Proc. of the ACM SIGPLAN'92 Conference on Programming Language Design and Implementation, pages 283-299 |
| | X | |

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.